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-- Company:

-- Engineer:

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-- Create Date: 13:28:38 01/16/2014

-- Design Name:

-- Module Name: one\_digit - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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**library** IEEE**;**

**use** IEEE**.**STD\_LOGIC\_1164**.ALL;**

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

**use** IEEE**.**NUMERIC\_STD**.ALL;**

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

**entity** one\_digit **is**

**Port** **(** DIGIT **:** **in** UNSIGNED **(**3 **downto** 0**);**

CATHODES **:** **out** STD\_LOGIC\_VECTOR **(**6 **downto** 0**));**

**end** one\_digit**;**

**architecture** Behavioral **of** one\_digit **is**

**begin**

**WITH** DIGIT **SELECT**

CATHODES **<=** "1000000" **WHEN** "0000"**,**

"1111001" **WHEN** "0001"**,**

"0100100" **WHEN** "0010"**,**

"0110000" **WHEN** "0011"**,**

"0011001" **WHEN** "0100"**,**

"0010010" **WHEN** "0101"**,**

"0000010" **WHEN** "0110"**,**

"1111000" **WHEN** "0111"**,**

"0000000" **WHEN** "1000"**,**

"0010000" **WHEN** "1001"**,**

"0111111" **WHEN** **OTHERS;**

**end** Behavioral**;**